

## AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A memory cell in an array of memory cells, said memory cell comprising:
  - a silicon substrate;
  - a floating gate formed at least in part within said silicon substrate; and
  - a bit line region in proximity to said floating gate, wherein said bit line region is enclosed within and surrounded by said silicon substrate ~~in proximity to said floating gate.~~
2. (Canceled).
3. (Original) The memory cell of Claim 1 wherein said bit line is formed in proximity to two adjacent surfaces of said floating gate.
4. (Original) The memory cell of Claim 3 wherein said bit line region is located below said floating gate and along one side of said floating gate.
5. (Original) The memory cell of Claim 1 further comprising:
  - a dielectric layer disposed over said floating gate; and
  - a control gate disposed over said oxide layer.
6. (Previously Presented) The memory cell of Claim 5 wherein said floating gate and said control gate comprise polysilicon, said bit line region comprises arsenic, and said dielectric layer comprises oxide-nitride-oxide.

7. (Previously Presented) The memory cell of Claim 1 further comprising:

a tunnel oxide layer formed between said silicon substrate and said floating gate.

8-14. (Canceled).

15. (Currently Amended) A flash memory array comprising:

a plurality of floating gates arrayed in rows and columns, said floating gates formed at least in part within a silicon substrate;

a control gate coupling floating gates and functioning as a word line; and

a plurality of bit lines, each bit line of said plurality of bit lines essentially perpendicular to said word line, wherein a length of said each bit line is completely buried within and surrounded by said substrate, said each bit line in cross-section having a first portion and a second portion that is essentially at a right angle to said first portion, wherein a first portion of a first bit line is essentially parallel to a first portion of a second bit line, wherein said first portion of said first bit line and said first portion of said second bit line lie in different planes, and wherein further a second portion of said first line and a second portion of said second bit line lie in essentially the same plane.

16. (Previously Presented) The flash memory array of Claim 15 wherein said each bit line is formed in proximity to two adjacent surfaces of said floating gates.

17. (Previously Presented) The flash memory array of Claim 16 wherein said each bit line is located below and along one side of a respective floating gate.

18. (Original) The flash memory array of Claim 15 further comprising: a dielectric layer formed between said control gate and said floating gates.

19. (Original) The flash memory array of Claim 18 wherein said oxide layer and said control gate are formed such that they separate adjacent floating gates along said word line.

20. (Previously Presented) The flash memory array of Claim 18 wherein said floating gates and said control gate comprise polysilicon, said bit lines comprise arsenic, and said dielectric layer comprises oxide-nitride-oxide.

21. (Original) The flash memory array of Claim 15 further comprising: a tunnel oxide layer formed between said substrate and said floating gates.

22. (New) The flash memory array of Claim 15 wherein said length of said each bit line is separated from said control gate by said substrate.